

## 200-mA LOW- $I_Q$ LOW-DROPOUT REGULATOR FOR PORTABLE DEVICES

 Check for Samples: [TLV70033-Q1](#), [TLV70025-Q1](#)

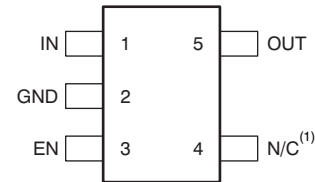
### FEATURES

- Qualified for Automotive Applications
- Very Low Dropout: 175 mV at 200 mA
- 2% Accuracy
- Low  $I_Q$ : 31  $\mu$ A
- Fixed-Output Voltage of 3.3 V
- High PSRR: 68 dB at 1 kHz
- Stable with Effective Capacitance of 0.1  $\mu$ F
- Thermal Shutdown and Overcurrent Protection
- Latch-Up Performance Meets 100 mA Per AEC-Q100, Level I
- Available in the SOT23-5 (DDC) Package

### APPLICATIONS

- MP3 Players
- ZigBee® Networks
- Bluetooth® Devices

DDC PACKAGE  
SOT23-5  
(TOP VIEW)

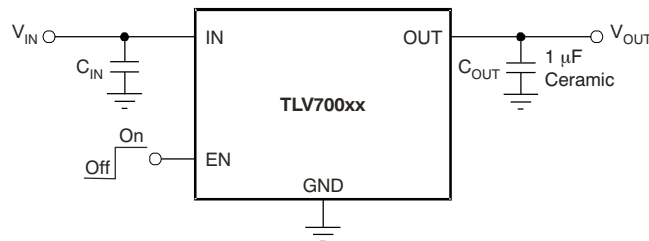


### DESCRIPTION

The TLV700xx series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1  $\mu$ F. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV700xx LDOs are available in the SOT23-5 (DDC) package.



Typical Application Circuit (Fixed-Voltage Versions)



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ZigBee is a registered trademark of ZigBee Alliance.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>J</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOT23 – DDC	Reel of 3000	TLV70033QDDCRQ1	OFL
			TLV70025QDDCRQ1	QVC

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

At T<sub>J</sub> = -40°C to 125°C (unless otherwise noted). All voltages are with respect to GND.

V <sub>IN</sub>	Input voltage range	-0.3 V to 6 V
V <sub>EN</sub>	Enable voltage range	-0.3 V to 6 V
V <sub>OUT</sub>	Output voltage range	-0.3 V to 6 V
I <sub>OUT</sub>	Maximum output current	Internally limited
	Output short-circuit duration	Indefinite
P <sub>D</sub>	Total continuous power dissipation	See <a href="#">Dissipation Ratings</a>
T <sub>J</sub>	Operating junction temperature range	-55°C to 150°C
T <sub>STG</sub>	Storage temperature range	-55°C to 150°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

**DISSIPATION RATINGS**

BOARD	PACKAGE	R <sub>θJC</sub>	R <sub>θJA</sub>	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> ≤ 25°C	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
Low-K <sup>(1)</sup>	DDC	90°C/W	280°C/W	3.6 mW/°C	360 mW	200 mW	145 mW
High-K <sup>(2)</sup>	DDC	90°C/W	200°C/W	5.0 mW/°C	500 mW	275 mW	200 mW

- (1) The JEDEC low-K (1s) board used to derive this data was a 3-inch x 3-inch, two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

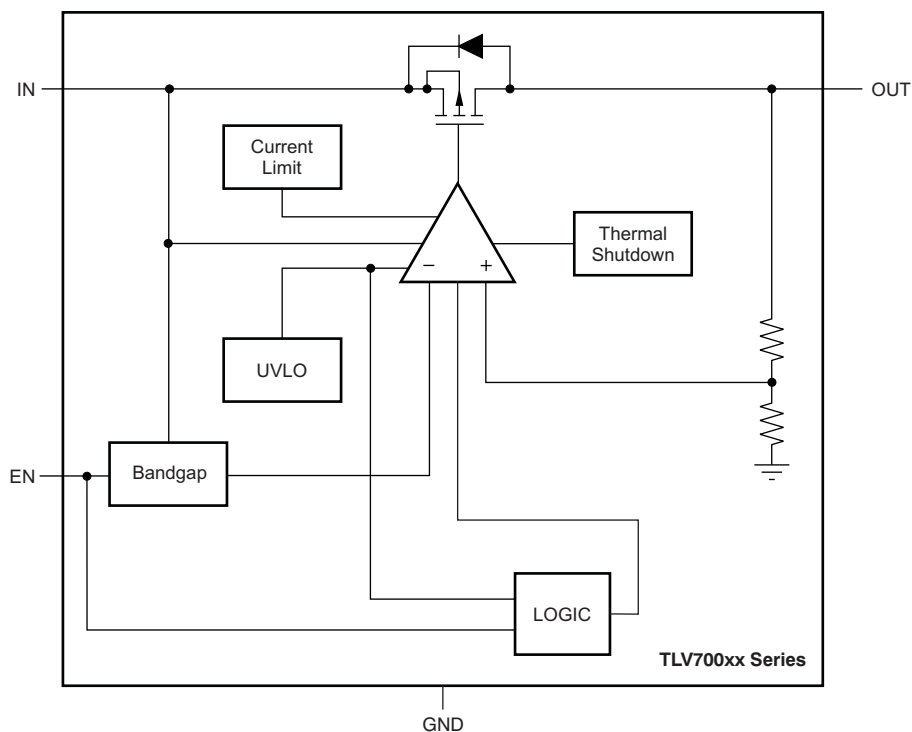
$V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$  or  $2.0\text{ V}$  (whichever is greater);  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\text{ }\mu\text{F}$ , and  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted). Typical values are at  $T_J = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS		TLV700xx			UNIT
				MIN	TYP	MAX	
$V_{IN}$	Input voltage range			2.0		5.5	V
$V_{OUT}$	DC output accuracy	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	$V_{OUT} \geq 1\text{ V}$	-2		+2	%
			$V_{OUT} < 1\text{ V}$	-20		20	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$			1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$			1	15	mV
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 200\text{ mA}$			175	250	mV
$I_{CL}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$		220	350	550	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{ mA}$			31	55	$\mu\text{A}$
		$I_{OUT} = 200\text{ mA}$ , $V_{IN} = V_{OUT} + 0.5\text{ V}$			270		$\mu\text{A}$
$I_{SHDN}$	Ground pin current (shutdown)	$V_{EN} \leq 0.4\text{ V}$ , $2.0\text{ V} \leq V_{IN} \leq 4.5\text{ V}$			1	2	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$V_{IN} = 2.3\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $f = 1\text{ kHz}$			68		dB
$V_N$	Output noise voltage	BW = 100 Hz to 100 kHz, $V_{IN} = 2.3\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 10\text{ mA}$			48		$\mu\text{V}_{RMS}$
$t_{STR}$	Startup time <sup>(2)</sup>	$C_{OUT} = 1.0\text{ }\mu\text{F}$ , $I_{OUT} = 200\text{ mA}$			100		$\mu\text{s}$
$V_{EN(HI)}$	Enable pin high (enabled)			0.9		$V_{IN}$	V
$V_{EN(LO)}$	Enable pin low (disabled)			0		0.4	V
$I_{EN}$	Enable pin current	$V_{EN} = 5.5\text{ V}$ , $I_{OUT} = 10\text{ }\mu\text{A}$			0.04	0.5	$\mu\text{A}$
UVLO	Undervoltage lockout	$V_{IN}$ rising			1.9		V
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing			160		$^\circ\text{C}$
		Reset, temperature decreasing			140		$^\circ\text{C}$
$T_J$	Operating junction temperature			-40		125	$^\circ\text{C}$

(1)  $V_{DO}$  is measured for devices with  $V_{OUT(NOM)} \geq 2.35\text{ V}$ .

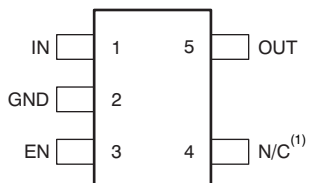
(2) Startup time = time from EN assertion to  $0.98 \times V_{OUT(NOM)}$ .

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATIONS

DDC PACKAGE  
SOT23-5  
(TOP VIEW)



### PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
IN	1	Input pin. A small 1- $\mu$ F ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See <a href="#">Input and Output Capacitor Requirements</a> in the <i>Application Information</i> section for more details.
GND	2	Ground pin
EN	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 $\mu$ A, nominal.
NC	4	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	Regulated output voltage pin. A small 1- $\mu$ F ceramic capacitor is needed from this pin to ground to assure stability. See <a href="#">Input and Output Capacitor Requirements</a> in the <i>Application Information</i> section for more details.

**TYPICAL CHARACTERISTICS**

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.0\text{ V}$  (whichever is greater);  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\ \mu\text{F}$  (unless otherwise noted). Typical values are at  $T_J = 25^{\circ}\text{C}$ .

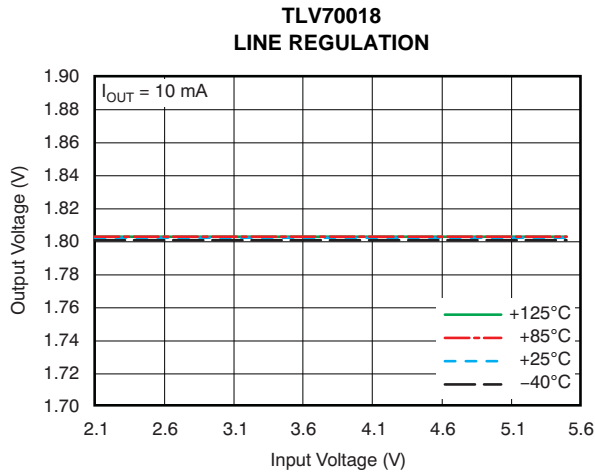


Figure 1.

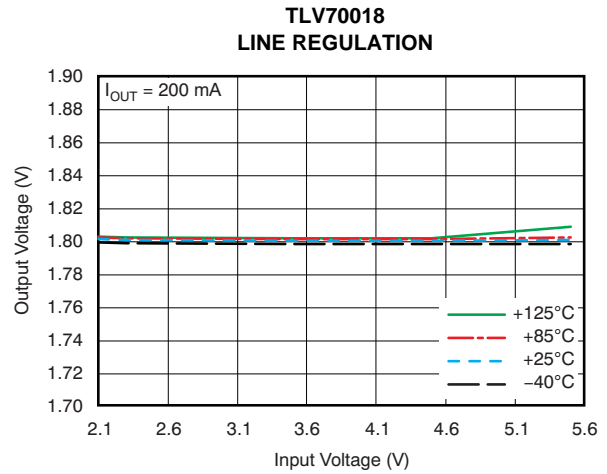


Figure 2.

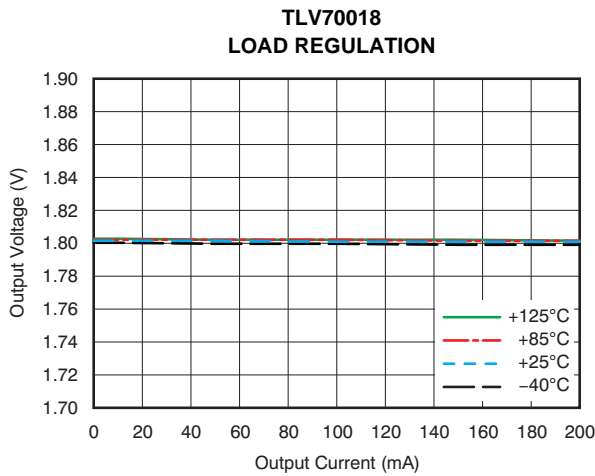


Figure 3.

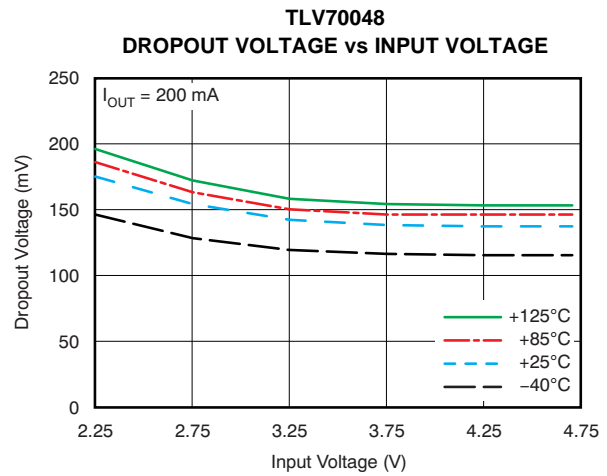


Figure 4.

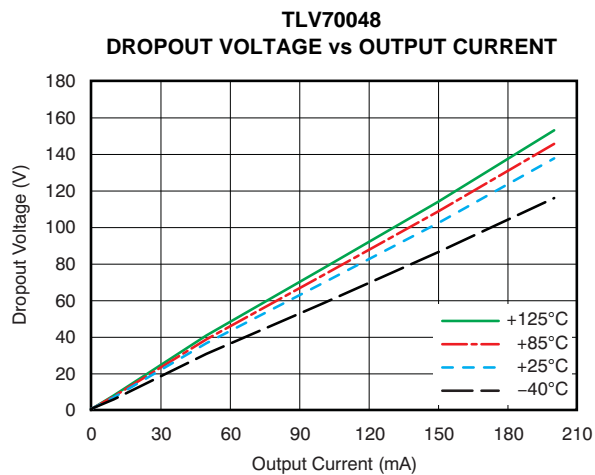


Figure 5.

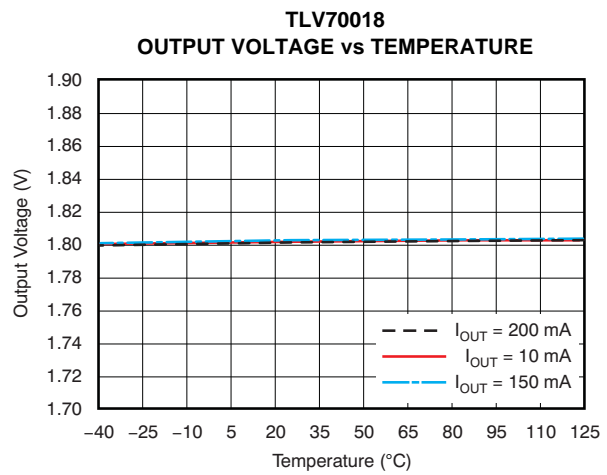
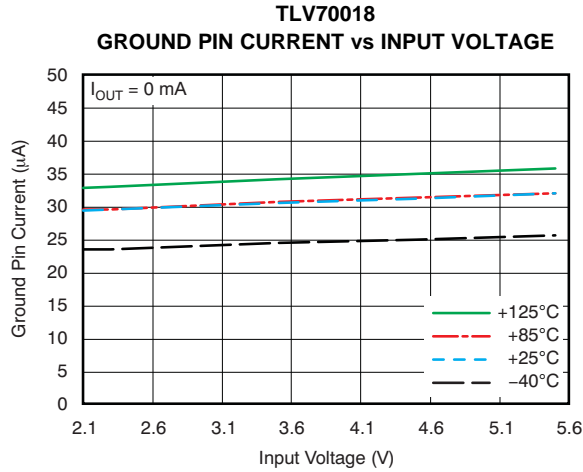


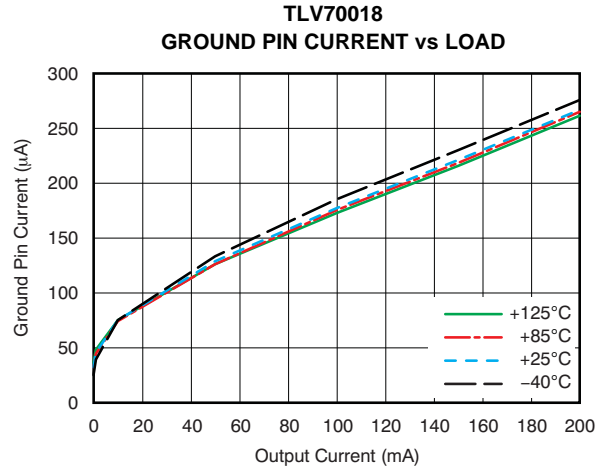
Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

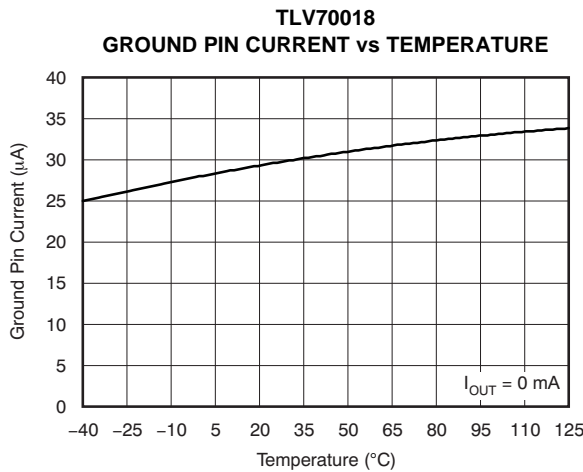
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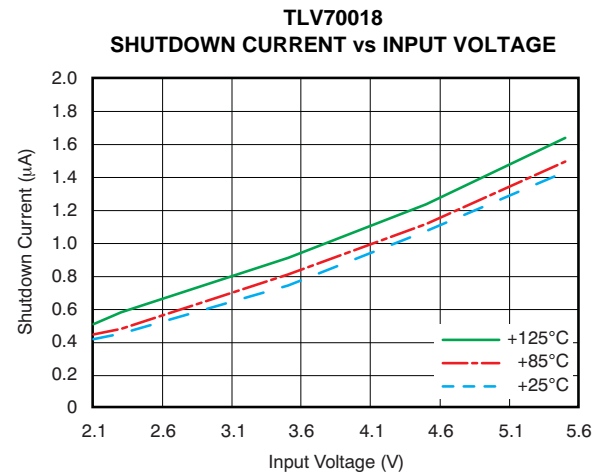
**Figure 7.**



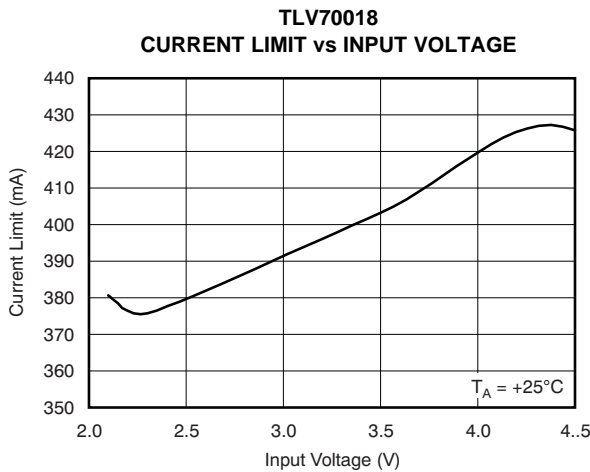
**Figure 8.**



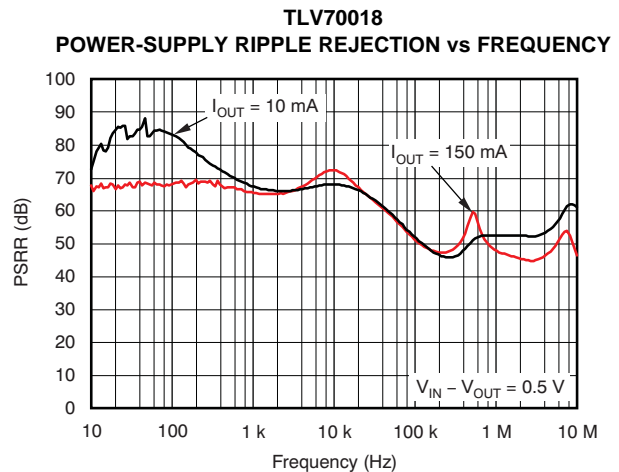
**Figure 9.**



**Figure 10.**



**Figure 11.**



**Figure 12.**

**TYPICAL CHARACTERISTICS (continued)**

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.0\text{ V}$  (whichever is greater);  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\text{ }\mu\text{F}$  (unless otherwise noted). Typical values are at  $T_J = 25^{\circ}\text{C}$ .

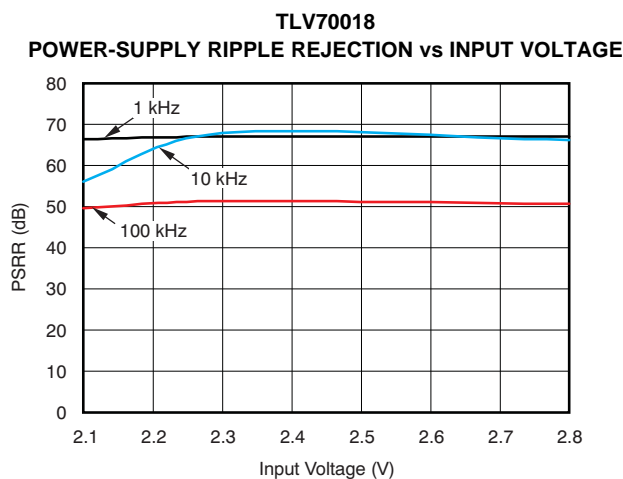


Figure 13.

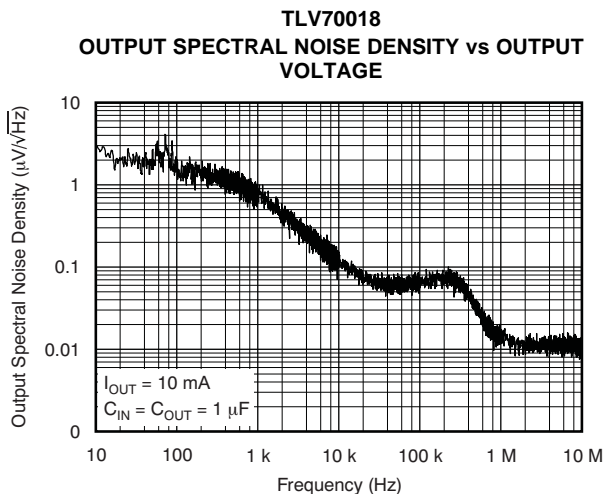


Figure 14.

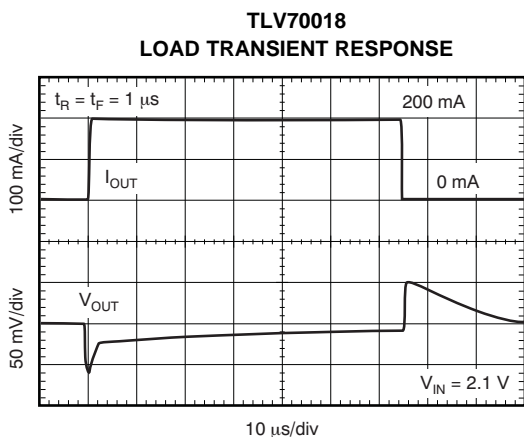


Figure 15.

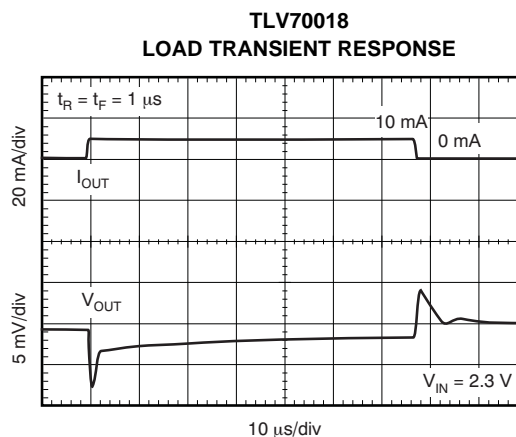


Figure 16.

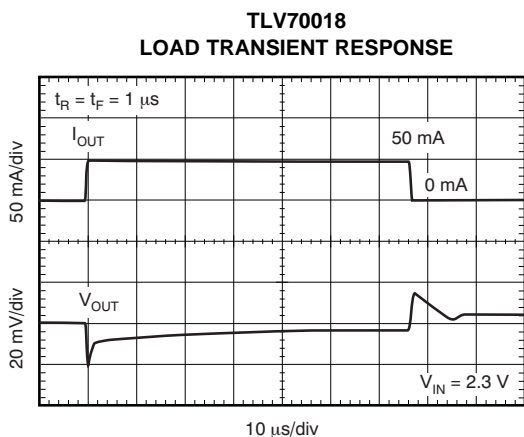


Figure 17.

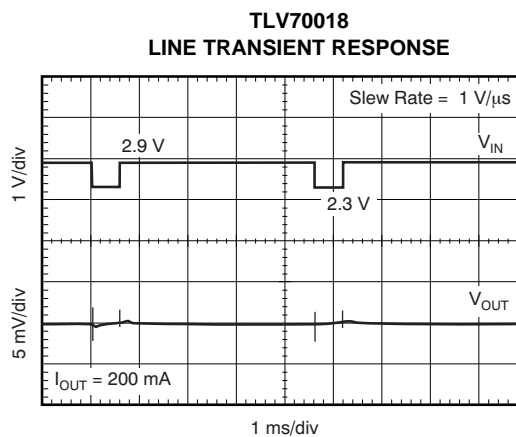
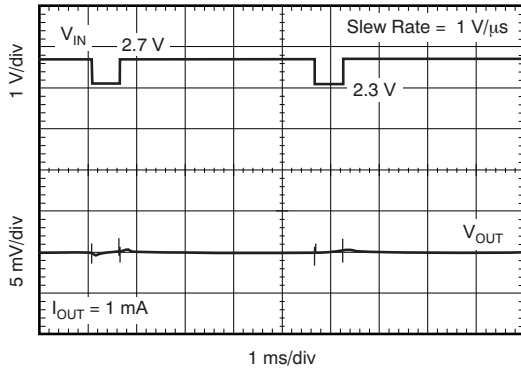


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

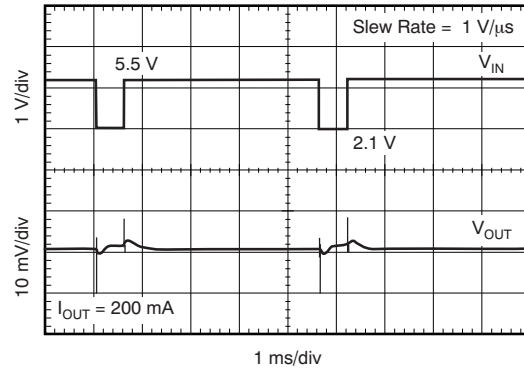
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**TLV70018**  
**LINE TRANSIENT RESPONSE**

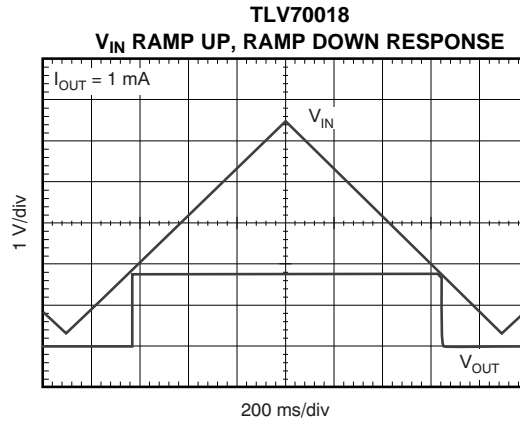


**Figure 19.**

**TLV70018**  
**LINE TRANSIENT RESPONSE**



**Figure 20.**



**Figure 21.**



## APPLICATION INFORMATION

The TLV700xx belongs to a new family of next-generation value LDO regulators. It consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little ( $V_{IN} - V_{OUT}$ ) headroom, make this device ideal for RF portable applications. This family of regulators offers sub-bandgap output voltages down to 0.7 V, current limit, and thermal protection, and is specified from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### Input and Output Capacitor Requirements

1.0- $\mu\text{F}$  X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700xx is designed to be stable with an *effective capacitance* of 0.1  $\mu\text{F}$  or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1  $\mu\text{F}$ . This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1- $\mu\text{F}$  effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Note that using a 0.1- $\mu\text{F}$  rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1  $\mu\text{F}$ . Maximum ESR should be less than 200 m $\Omega$ .

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- $\mu\text{F}$  to 1.0- $\mu\text{F}$ , low ESR capacitor across the IN pin and GND in of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2  $\Omega$ , a 0.1- $\mu\text{F}$  input capacitor may be necessary to ensure stability.

### Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

### Internal Current Limit

The TLV700xx internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is  $V_{OUT} = I_{LIMIT} \times R_{LOAD}$ . The PMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{LIMIT}$  until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Information](#) section for more details.

The PMOS pass element in the TLV700xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

### Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

### Dropout Voltage

The TLV700xx uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in [Figure 13](#) in the [Typical Characteristics](#) section.

## Transient Response

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

## Undervoltage Lockout (UVLO)

The TLV700xx uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

## Thermal Information

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV700xx into thermal shutdown degrades device reliability.

## Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the [Dissipation Ratings](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TLV70025QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
TLV70033QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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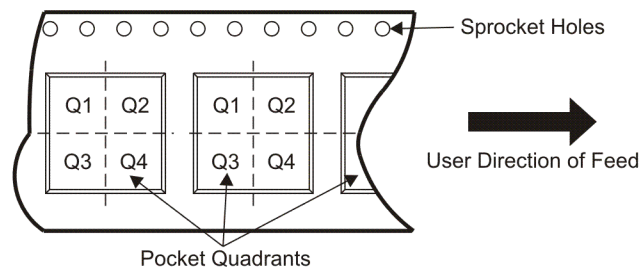
**OTHER QUALIFIED VERSIONS OF TLV70025-Q1, TLV70033-Q1 :**

- Catalog: [TLV70025](#), [TLV70033](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70025QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

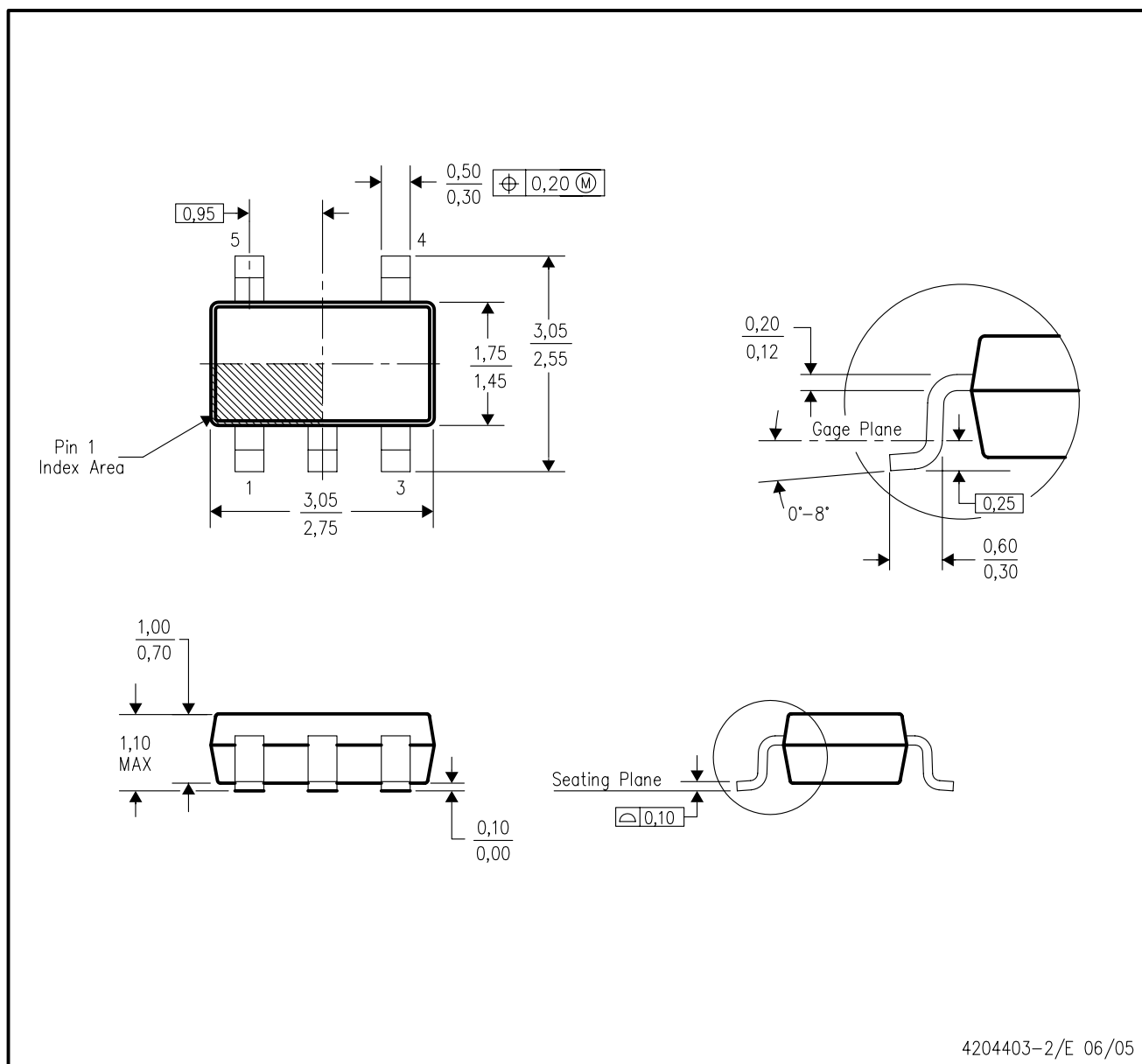
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70025QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70033QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0

DDC (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-193 variation AB (5 pin).

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
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