SCAN921260

SCAN921260 X6 1:10 Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST

TEXAS INSTRUMENTS

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X6 1:10 Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST

General Description

The SCAN921260 integrates six deserializer devices into a single chip. The SCAN921260 can simultaneously deserialize up to six data streams that have been serialized by the National Semiconductor SCAN921023 Bus LVDS serializer. The device also includes a seventh serial input channel that serves as a redundant input.

Each deserializer block in the SCAN921260 operates independently with its own clock recovery circuitry and lock-detect signaling.

The SCAN921260 uses a single +3.3V power supply with an estimated power dissipation of 1.2W at 3.3V with a PRBS-15 pattern. Refer to the Connection Diagrams for packaging information.

Features

- IEEE 1149.1 (JTAG) Compliant and at-speed BIST test modes
- Deserializes one to six BusLVDS input serial data streams with embedded clocks
- Seven selectable serial inputs to support n+1 redundancy of deserialized streams
- Seventh channel has single pin monitor output that reflects input from seventh channel input
- Parallel clock rate up to 66MHz
- On chip filtering for PLL
- High impedance inputs upon power off (V_{cc} = 0V)
- Single power supply at +3.3V
- 196-pin LBGA package (Low-profile Ball Grid Array) package
- Industrial temperature range operation: −40 to +85

Functional Block Diagram

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TRI-STATE® is a registered trademark of National Semiconductor Corporation.
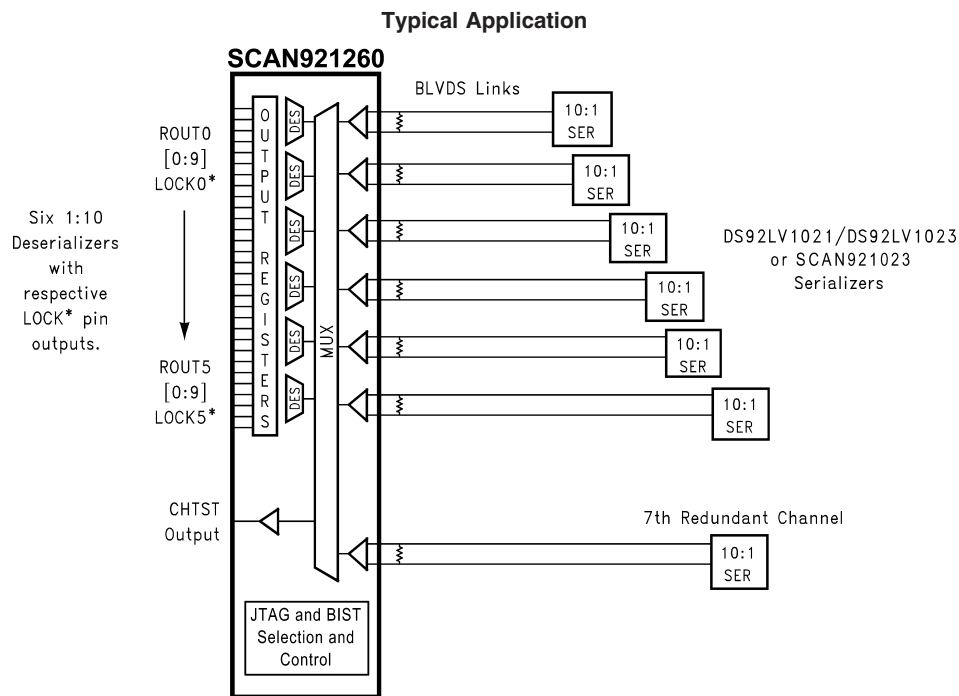
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage	−0.3V to 3.9V
LVCMOS/LVTTL Output Voltage	−0.3V to 3.9V
Bus LVDS Receiver Input Voltage	−0.3V to 3.9V
Bus LVDS Driver Output Voltage	−0.3V to 3.9V
Bus LVDS Output Short Circuit Duration	10ms
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 10 seconds)	+225˚C

Max Pkg Power Dissipation Capacity @ 25˚C

196L BGA	3.7 W

Package Derating:

196L BGA	29.4 mW/˚C above +25˚C

Thermal Resistance:

θ_{JA}	34˚C/W
θ_{JC}	8˚C/W

ESD Rating:

Human Body Model	>2KV
Machine Model	>750V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C
Clock Rate	20		66	MHz

Electrical Characteristics
Over recommended operating supply and temperature ranges unless otherwise specified(Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS/LVTTL DC Specifications: Applies to pins in Pin Description table with type CMOS Input or Output						
V_{IH}	High Level Input Voltage	Input Pins	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage	Input Pins	GND		0.8	V
V_{CL}	Input Clamp Voltage	Input Pins		-0.87	-1.5	V
I_{IN}	Input Current	V_{in} = 0 or 3.6, Input Pins	-20		+20	uA
V_{OH}	High Level Output Voltage	I_{OH} = 6mA, Output Pins	2	3	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 6mA, Output Pins	GND	0.18	0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = 12mA, TDO Output	2	3	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 12mA, TDO Output	GND	0.18	0.4	V
I_{OS}	Output short Circuit Current	V_{out} = 0V, Output Pins	-15	-46	-85	mA
I_{OS}	Output short Circuit Current	V_{out} = 0V, TDO Output	-15		-120	mA
I_{OZ}	TRI-STATE Output Current	PD* or REN = 0.8V V_{out} = 0V or V_{CC}	-10	+/-0.2	+10	uA
Bus LVDS DC specifications: Applies to pins in Pin Description table with type Bus LVDS Inputs						
V_{TH}	Differential Threshold High Voltage	VCM = 1.1V (V_{RI+}-V_{RI-})		+3	+50	mV
V_{TL}	Differential Threshold Low Voltage		-50	-2		mV
I_{IN}	Input Current	V_{in} = +2.4V or 0V, V_{cc} = 3.6 or 0V	-10	+/- 1	+10	uA
Supply Current						
I_{CCR}	Worst Case Supply Current	3.6V, Checker Board Pattern, C_L = 15pF, 66Mhz		600	660	mA
I_{CCXR}	Supply Current when Powered Down	$\overline{PWRDN}$= 0.8V REN = 0.8V		0.36	1	mA

Electrical Characteristics Over recommended operating supply and temperature ranges unless otherwise specified(Note 2) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Timing Requirements for REFCLK							
t_{RFCP}	REFCLK Period			15.15		50	ns
t_{RFDC}	REFCLK Duty Cycle			40	50	60	%
t_{RFCP}/t_{TCP}	Ratio of REFCLK to TCLK			0.95		1.05	
t_{RFTT}	REFCLK Transition Time					8	ns
Deserializer Switching Characteristics							
t_{RCP}	RCLK Period	RCLK		15.15		50	ns
t_{RDC}	RCLK Duty Cycle	RCLK (Note 7)		45	50	55	%
t_{CHTST}	Period of Bus LVDS signal when CHTST is selected by MUX	CHTST (Note 6)		25			ns
t_{CLH}	CMOS/TTL Low-to-High Transition Time	C_L = 15pF			1.7	6	ns
t_{CHL}	CMOS/TTL High-to-Low Transition Time	C_L = 15pF			1.6	6	ns
t_{ROS}	Rout Data Valid before RCLK	C_L = 15pF, *Figure 2*		$0.35*t_{RCP}$			ns
t_{ROH}	Rout Data Valid after RCLK	C_L = 15pF, *Figure 2*		$-0.35*t_{RCP}$			ns
t_{HZR}	High to TRI-STATE Delay	C_L = 15pF, *Figure 7*				12	ns
t_{LZR}	Low to TRI-STATE Delay					12	ns
t_{ZHR}	TRI-STATE to High Delay					12	ns
t_{ZLR}	TRI-STATE to Low Delay					12	ns
t_{DD}	Deserializer Delay	*Figure 1*		$1.75*t_{RCP}$ +3	$1.75*t_{RCP}$ +7	$1.75*t_{RCP}$ +10.5	ns
t_{DSR1}	Deserializer PLL LOCK Time from PWRDN (with SYNCPAT)	*Figure 3* (Note 4)	66Mhz			2	us
			20Mhz			10	us
t_{DSR2}	Deserializer PLL Lock Time from SYNCPAT	*Figure 4* (Note 4)	66Mhz			1.5	us
			20Mhz			5	us
t_{RNMI-R}	Ideal Strobe Window Right	66Mhz, *Figure 10*				+400	ps
t_{RNMI-L}	Ideal Strobe Window Left	66Mhz, *Figure 10*		-400			ps

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Typical values are given for Vcc = 3.3V and TA =25˚C

Note 3: Current into the device pins is defined as positive. Current out of device pins is defined as negative. Voltage are referenced to ground except VOD, VTH and VTL which are differential voltages.

Note 4: For the purpose of specifying deserializer PLL performance t_{DSR1} and t_{DSR2} are specified with the REFCLK running and stable, and specific conditions of the incoming data stream (SYNCPATs). t_{DSR1} is the time required for the deserializer to indicate lock upon power-up or when leaving the power-down mode. t_{DSR2} is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI−) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). The time to lock to random data is dependent upon the incoming data.

Note 5: t_{RNM} is a measure of how much phase noise (jitter)the deserializer can tolerate in the incoming data stream before bit errors occur. The Deserializer Noise Margin is Guaranteed By Design (GBD) using statistical analysis.

Note 6: Because the Bus LVDS serial data stream is not decoded, the maximum frequency of the CHTST output driver could be exceeded if the data stream were switched to CHTST. The maximum frequency of the BUS LVDS input should not exceed the parallel clock rate.

Note 7: Guaranteed By Design (GBD) using statistical analysis.

SCAN Circuitry Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum TCK Clock Frequency	$R_L = 500\Omega$, $C_L = 35$ pF	25.0	50.0		MHz
t_S	TDI to TCK, H or L		1.0			ns
t_H	TDI to TCK, H or L		2.0			ns
t_S	TMS to TCK, H or L		2.5			ns
t_H	TMS to TCK, H or L		1.5			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{TRST}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{TRST}$ to TCK		2.0			ns

Block Diagram
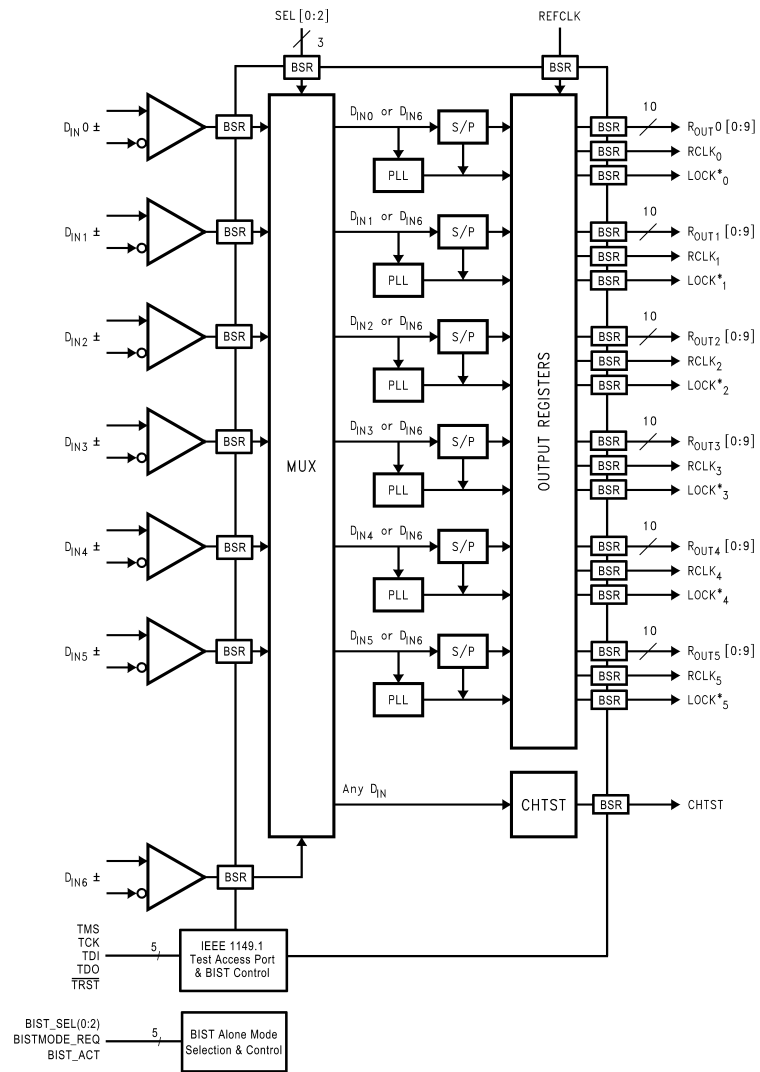
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Control Pins Truth Table

PWRDN	REN	SEL2	SEL1	SEL0	Rout	CHTST	LOCK[0:5]	RCLK[0:5]
H	H	L	L	L	Din6 Decoded to Rout 0 (0:9)(Note 11)	Din0 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
H	H	L	L	H	Din6 Decoded to Rout 1 (0:9)(Note 11)	Din1 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
H	H	L	H	L	Din6 Decoded to Rout 2 (0:9)(Note 11)	Din2 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
H	H	L	H	H	Din6 Decoded to Rout 3 (0:9)(Note 11)	Din3 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
H	H	H	L	L	Din6 Decoded to Rout 4 (0:9)(Note 11)	Din4 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
H	H	H	L	H	Din6 Decoded to Rout 5 (0:9)(Note 11)	Din5 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
H	H	H	H	L	Din6 is not Decoded	Z	Active(Note 9)	Active(Notes 10, 11)
H	H	H	H	H	Din6 is not Decoded	Din6 (not decoded)	Active(Note 9)	Active(Notes 10, 11)
L	X	X	X	X	Z	Z	Z	Z
H	L	X	X	X	Z	Z	Active(Note 9)	Z

Note 8: The routing of the Din inputs to the Deserializers and to the CHTST outputs are dependent on the states of SEL [0:2].

Note 9: $\overline{LOCK}$ Active indicates that the $\overline{LOCK}$ output will reflect the state of it's respective Deserializer with regard to the selected data stream.

Note 10: RCLK Active indicates that the RCLK will be running if the Deserializer is locked.

Note 11: Rout n[0:9] and RCLK [0:5] are Tri-Stated when $\overline{LOCKn}$[0:5] is High.

Timing Diagrams
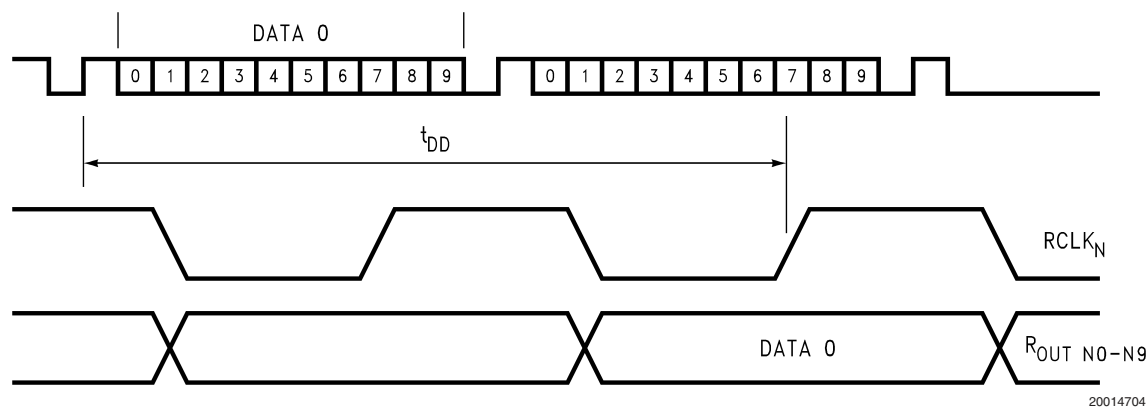
FIGURE 1. Deserializer Delay t_{DD}

Timing Diagrams (Continued)
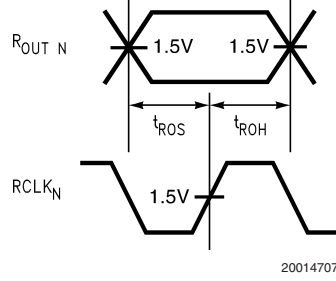
FIGURE 2. Output Timing t_{ROS} and t_{ROH}
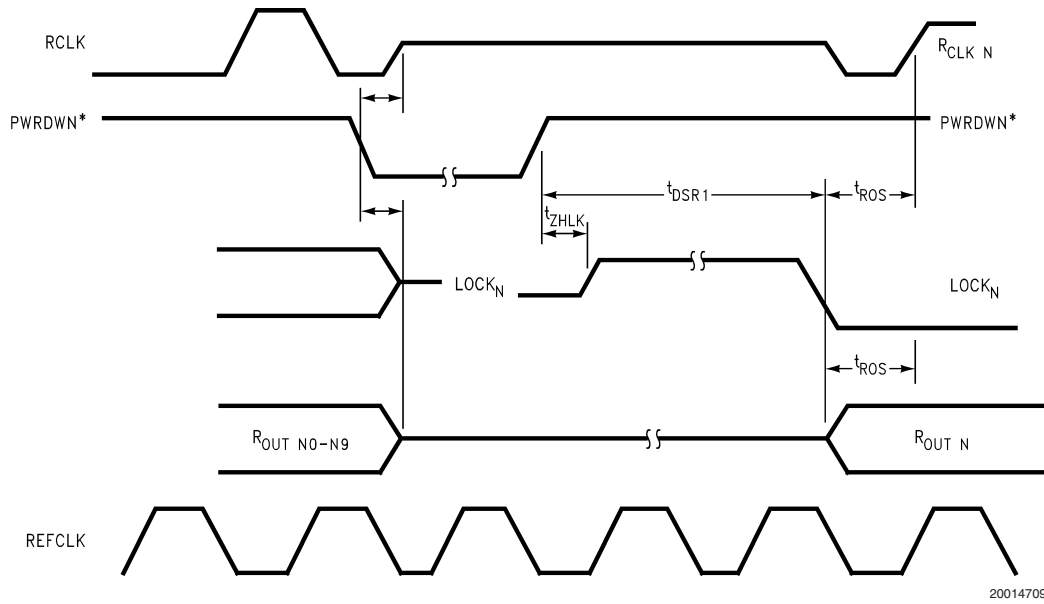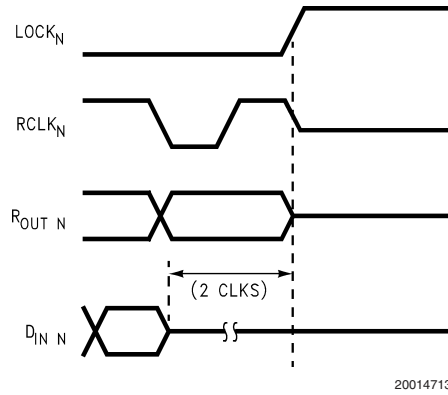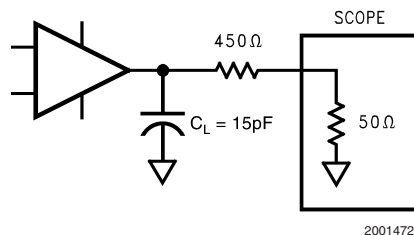

FIGURE 3. Locktime from PWRDN* t_{DSR1}
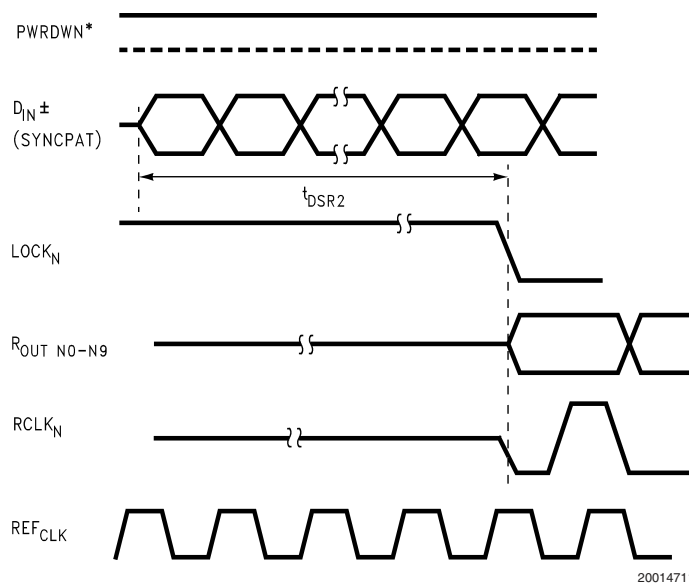
FIGURE 4. Locktime to SYNCPAT t_{DSR2}
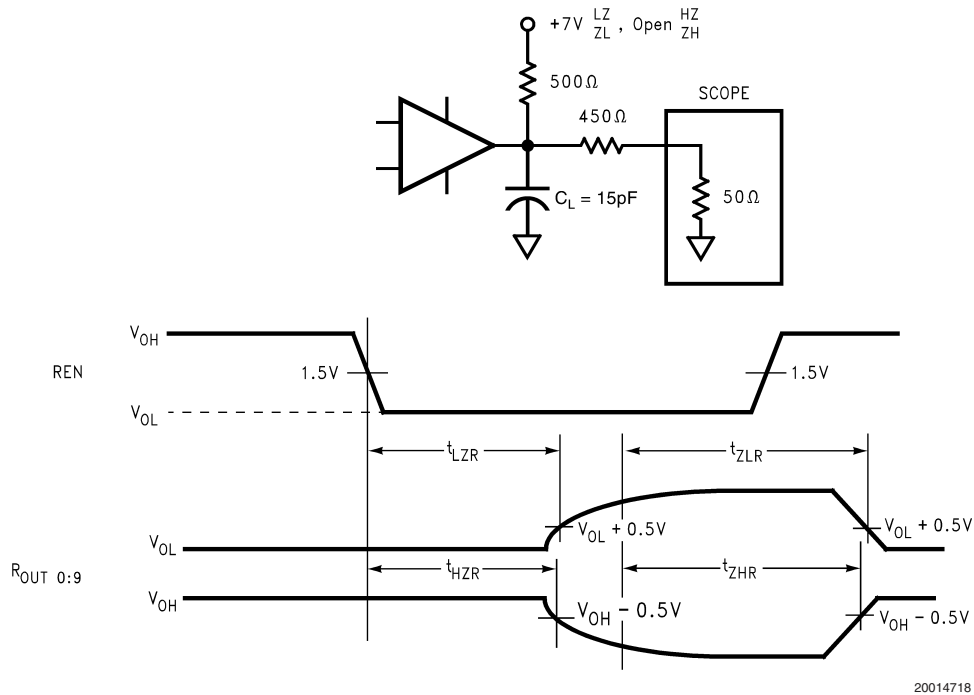
Timing Diagrams (Continued)

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FIGURE 5. Unlock

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Note: C_L includes Jig and stray capacitance. For the TDO output, $C_L = 35pF$.

FIGURE 6. Output load for Timing and Switching Characteristics

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Note: C_L includes Jig and stray capacitance. For the TDO output, $C_L = 35pF$.

FIGURE 7. Deserializer TRI-STATE Test Circuit and Timing

Application Information

USING THE SCAN921023 and SCAN921260

The SCAN921260 combines six 1:10 deserializers into a single chip. Each of the six deserializers accepts a BusLVDS data stream up to 660 Mbps from National Semiconductor's SCAN921023 Serializer. The deserializers then recover the embedded two clock bits and data to deliver the resulting 10-bit wide words to the output. A seventh serial data input provides n+1 redundancy capability. The user can program the seventh input to be an alternative input to any of the six deserializers. Whichever input is replaced by the seventh input is then routed to the CHANNEL TEST (CHTST) pin on receiver output port. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the $\overline{\text{LOCKn}}$ output high when loss of lock occurs.

Each of the 6 channels acts completely independent of each other. Each independent channel has outputs for a 10-bit wide data word, the recovered clock out, and the lock-detect output.

The SCAN921260 has three operating states: Initialization, Data Transfer, and Resynchronization. In addition, there are two passive states: Powerdown and TRI-STATE.

The following sections describe each operating mode and passive state.

INITIALIZATION

Before the SCAN921260 receives and deserializes data, it and the transmitting serializer devices must initialize the link. Initialization refers to synchronizing the Serializer's and the Deserializer's PLL's to local clocks. The local clocks must be the same frequency or within a specified range if from different sources. After all devices synchronize to local clocks, the Deserializers synchronize to the Serializers as the second and final initialization step.

Step 1: After applying power to the Deserializer, the outputs are held in TRI-STATE and the on-chip power-sequencing circuitry disables the internal circuits. When V_{cc} reaches V_{cc}OK (2.1V), the PLL in each deserializer begins locking to the local clock (REFCLK). A local on-board oscillator or other source provides the specified clock input to the REFCLK pin.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. Refer to the Serializer data sheet for the proper operation during this step of the Initialization State. The Deserializer identifies the rising clock edge in a synchronization pattern or random data and after 80 clock cycles will synchronize to the data stream from the serializer. At the point where the Deserializer's PLL locks to the embedded clock, the $\overline{\text{LOCKn}}$ pin goes low and valid data appears on the output. Note that this differs from previous deserializers where the $\overline{\text{LOCKn}}$ signal was not synchronous to valid data appearing on the outputs.

DATA TRANSFER

After initialization, the serializer transfers data to the deserializers. The serial data stream includes a start and stop bit appended by the serializer, which frame the ten data bits. The start bit is always high and the stop bit is always low. The start and stop bits also function as clock bits embedded in the serial stream.

The Serializer transmits the data and clock bits (10+2 bits) at 12 times the TCLK frequency. For example, if TCLK is 40

MHz, the serial rate is 40 X 12 = 480 Mbps. Since only 10 bits are from input data, the serial 'payload' rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data is 40 X 10 = 400 Mbps. TCLK is provided by the data source and must be in the range 20 MHz to 40 MHz nominal.

When one of six Deserializer channels synchronizes to the input from a Serializer, it drives its $\overline{\text{LOCKn}}$ pin low and synchronously delivers valid data on the output. The Deserializer locks to the embedded clock, uses it to generate multiple internal data strobes, and drives the embedded clock to the RCLKn pin. The RCLKn is synchronous to the data on the ROUT[n0:n9] pins. While $\overline{\text{LOCKn}}$ is low, data on ROUT [n0:n9] is valid. Otherwise, ROUT[n0:n9] is invalid.

All ROUT, $\overline{\text{LOCK}}$, and RCLK signals will drive a minimum of three CMOS input gates (15pF load) with a 66 MHz clock. This amount of drive allows bussing outputs of two Deserializers and a destination ASIC. REN controls TRI-STATE of all the outputs.

The Deserializer input pins are high impedance during Powerdown ($\overline{\text{PWRDN}}$ low) and power-off (V_{cc} = 0V).

RESYNCHRONIZATION

Whenever one of the six Deserializers loses lock, it will automatically try to resynchronize. For example, if the embedded clock edge is not detected two times in succession, the PLL loses lock and the $\overline{\text{LOCKn}}$ pin is driven high. The system must monitor the $\overline{\text{LOCKn}}$ pin to determine when data is valid.

The user has the choice of allowing the deserializer to resynch to the data stream or to force synchronization by pulsing the Serializer SYNC1 or SYNC2 pin. This scheme is left up to the user discretion. One recommendation is to provide a feedback loop using the $\overline{\text{LOCKn}}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are given for multiple control in a multi-drop application.

POWERDOWN

The Powerdown state is a low power sleep mode that the Serializer and Deserializer typically occupy while waiting for initialization, or to reduce power consumption when no data is transferred. The Deserializer enters Powerdown when $\overline{\text{PWRDN}}$ is driven low. In Powerdown, the PLL stops and the outputs go into TRI-STATE, which reduces supply current to the microamp range. To exit Powerdown, the system drives $\overline{\text{PWRDN}}$ high.

Upon exiting Powerdown, the Deserializer enters the Initialization state. The system must then allow time to Initialize before data transfer can begin.

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When the system drives REN pin low, the Deserializer enters TRI-STATE. This will TRI-STATE the receiver output pins (ROUT[00:59]) and RCLK[0:5]. When the system drives REN high, the Deserializer will return to the previous state as long as all other control pins remain static ($\overline{\text{PWRDN}}$).

IEEE 1149.1 TEST MODES

The SCAN921260 features interconnect test access that is compliant to the IEEE 1149.1 Standard for Boundary Scan Test (JTAG). All digital TTL I/O's on the device are accessible using IEEE 1149.1, and entering this test mode will override

Application Information   (Continued)

all input control cases including $\overline{PWRDN}$ and REN. In addition to the 4 required Test Access Port (TAP) signals of TMS, TCK, TDI, and TDO, $\overline{TRST}$ is provided for test reset.

To supplement the test coverage provided by the IEEE 1149.1 test access to the digital TTL pins, the SCAN921260 has two instructions to test the LVDS interconnects. The first is EXTEST. This is implemented at LVDS levels and is only intended as a go no-go test (e.g. missing cables). The second method is the RUNBIST instruction. It is an "at-system-speed" interconnect test. It is executed in approximately 33mS with a system clock speed of 66MHz. There are 12 bits in the RX BIST data register for notification of PASS/FAIL and TEST_COMPLETE; two bits for each of the six channels. The RX BIST register is defined as (from MSB to LSB):

[BIST COMPLETE for Channel 6, BIST PASS/FAIL for Channel 6, BIST COMPLETE for Channel 5, BIST PASS/FAIL for Channel 5, BIST COMPLETE for Channel 4, BIST PASS/FAIL for Channel 4, BIST COMPLETE for Channel 3, BIST PASS/FAIL for Channel 3, BIST COMPLETE for Channel 2, BIST PASS/FAIL for Channel 2, BIST COMPLETE for Channel 1, BIST PASS/FAIL for Channel 1]

A "pass" indicates that the BER (Bit-Error-Rate) is better than 10^{-7}. This is a minimum test, so a "fail" indication means that the BER is higher than 10^{-7}.

The BIST features of the SCAN921260 six (6) channel de-serializer are compatible with the BIST features on the SCAN921023 Serializer.

An important detail is that once both devices have the RUNBIST instruction loaded into their respective instruction registers, both devices must move into the RTI state within 4K system clocks (At a system CLK of 66Mhz and TCK of 1MHz this allows for 66 TCK cycles). This is not a concern when both devices are on the same scan chain or LSP, however, it can be a problem with some multi-drop devices. This test mode has been simulated and verified using National's SCANSTA111.

Typical applications of 1149.1 are based around TTL-type inputs. With the introduction of 1149.1 into LVDS there have been many hurdles to overcome. One issue is that TTL inputs and outputs do not require bias circuits and are always on when power is applied. In the case of LVDS, there are many circuits required to make the inputs and outputs achieve their tight tolerances. These circuits require settle time once power is applied to ensure they function properly. These circuits are also the largest users of power within the device. To reduce power in standby, these devices have a $\overline{PWRDN}$ pin to shut these circuits down. There is also a REN pin that enables/disables the TTL outputs.

In the case of the 1149.1 functionality, these circuits need appropriate time to stabilize before they can be utilized. To achieve stability, these circuits are powered up when the TAP controller state machine is not in the *Test-Logic-Reset* state. The time that it takes a TAP to traverse from *Test-Logic-Reset* to *Capture-Data-Register* running at 25MHz is sufficient to allow these circuits to stabilize.

Once the TAP has left *Test-Logic-Reset*, the internal value of $\overline{PWRDN}$ is overridden and the device is powered up. This includes all fore mentioned circuits as well as all outputs. If an application requires that the outputs are to remain disabled during 1149.1 test, use REN and not $\overline{PWRDN}$.

KNOWN ERRATA: On the SCAN921260 only the overridden value of $\overline{PWRDN}$ ("1") is captured during all 1149.1 tests and not the external value as seen on the pin.

BIST ALONE TEST MODES

The SCAN921260 also supports a BIST Alone feature which can be run without enabling the JTAG TAP controller. This feature provides the ability to run continuos BER testing on all channels, or on individual channels without affecting live traffic on other channels. The ability to run the BERT while adjacent channels are carrying normal traffic is a useful tool to determine how normal traffic will affect BER on any given channel.

The BIST Alone features can be accessed using the 5 pins defined as BIST_SEL0, BIST_SEL1, BIST_SEL2, BIST_ACT, and BISTMODE_REQ.

BIST_ACT activates the BIST Alone mode. The BIST Alone mode will continue until deactivated by the BIST_ACT pin. The BIST_ACT input must be high or low for 4 or more clock cycles in order to activate or deactivate the BIST Alone mode. The BIST_ACT input is pulled low internally.

BISTMODE_REQ is used to select either gross error reporting or a specific output error report. When the BIST Alone mode is active, the $\overline{LOCK(1:6)}$ output for all channels running BIST Alone will go low, and ROUT(0:9) reports any error. When BISTMODE_REQ is low the error reporting is set to Gross Mode, and whenever a bit contains one or more errors, ROUT(0:9) for that channel goes high and stays high until deactivation by the BIST_ACT input. When BISTMODE_REQ is high, the output error reporting is set to Bit Error mode. Whenever any data bit contains an error, the data output for that corresponding bit goes high. The default is Gross Error mode.

The three BIST_SELn inputs determine which channel is in BIST Alone mode according to the following table:

Application Information (Continued)

BIST Alone Mode Selection

BIST_ACT	BIST_SEL2	BIST_SEL1	BIST_SEL0	BIST for Channel
1	0	0	0	0
1	0	0	1	1
1	0	1	0	2
1	0	1	1	3
1	1	0	0	4
1	1	0	1	5
1	1	1	0	All Channels
1	1	1	1	IDLE
0	X	X	X	IDLE

POWER CONSIDERATIONS

An all CMOS design of the Deserializer makes it an inherently low power device.

POWERING UP THE DESERIALIZER

The SCAN921260 can be powered up at any time by following the proper sequence. The REFCLK input can be running before the Deserializer powers up, and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs will remain in TRI-STATE until the Deserializer detects data transmission at its inputs and locks to the incoming data stream.

TRANSMITTING DATA

Once you power up the Deserializer, it must be phase locked to the transmitter to transmit data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends sync patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The $\overline{\text{LOCKn}}$ output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the $\overline{\text{LOCKn}}$ output of the Deserializer to one of the SYNC inputs of the Serializer will guarantee that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the "random lock" circuitry to find and lock to the data stream.

While the Deserializer $\overline{\text{LOCKn}}$ output is low, data at the Deserializer outputs (ROUT0-9) are valid, except for the specific case of loss of lock during transmission which is further discussed in the "Recovering from LOCK Loss" section below.

NOISE MARGIN

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)

Media: ISI, Large V_{CM} shifts

Deserializer: V_{CC} noise

RECOVERING FROM LOCK LOSS

In the case where the Deserializer loses lock during data transmission, up to 1 cycle of data that was previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 2 times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. Therefore, after the Deserializer relocks to the incoming data stream and the Deserializer $\overline{\text{LOCKn}}$ pin goes low, at least one previous data cycle should be suspect for bit errors.

The Deserializer can relock to the incoming data stream by making the Serializer resend SYNC patterns, as described above, or by random locking, which can take more time, depending on the data patterns being received.

HOT INSERTION

All the BusLVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in *Figure 10*.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the SCAN921260 should be designed to provide noise-free power to the device. Good layout practice will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. There are a few common practices which should be followed when designing PCB's for Bus LVDS Signaling. Recommended layout practices are:

- Use at least 4 PCB board layers (Bus LVDS signals, ground, power, and TTL signals).

  Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical.

- Keep Serializers and Deserializers as close to the (Bus LVDS port side) connector as possible.

  Longer stubs lower the impedance of the bus, increase the load on the Serializer, and lower the threshold margin at the Deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the Serializer Bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.

Application Information (Continued)

- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes.

  Surface mount capacitors placed close to power and ground pins work best. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.001 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. Randomly distributed by-pass capacitors should also be used.

  Package and pin layout permitting, it is also recommended to use two vias at each power pin as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance between layers by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

- Leave unused Bus LVDS receiver inputs open (floating).
- Isolate TTL signals from Bus LVDS signals.

There are more common practices which should be followed when designing PCBs for BLVDS/LVDS signaling. General application guidelines are available in the LVDS Owner's Manual (www.national.com/lvds). For packaging information on BGA's, please see AN-1126.

TRANSMISSION MEDIA

The Serializer and Deserializer can also be used in point-to-point configurations, through PCB trace, or through twisted pair cable. In point-to-point configurations, the transmission media need only be terminated at the receiver end. Please note that in point-to-point configurations, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Also, Bus LVDS provides a +/− 1.2V common mode range at the receiver inputs.

FAILSAFE BIASING FOR THE SCAN921260

The SCAN921260 has internal failsafe biasing and an improved input threshold sensitivity of +/− 50mV versus +/− 100mV for the DS92LV1210 or DS92LV1212. This allows for greater differential noise margin in the SCAN921260. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the SCAN921260 can pickup noise as a signal and cause unintentional locking. For example, this can occur when the input cable is disconnected.

External resistors can be added to the receiver circuit board to prevent noise pick-up. Typically, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. The pull-up and pull-down resistors (R_1 and R_2) provide a current path through the termination resistor (R_L) which biases the receiver inputs when they are not connected to an active driver. The value of the pull-up and pull-down resistors should be chosen so that enough current is drawn to provide a +15mV drop across the termination resistor. Please see *Figure 8* for the Failsafe Biasing Setup.

The parameter t_{RNM} is calculated by first measuring how much of the ideal bit the receiver needs to ensure correct sampling. After determining this amount, what remains of the ideal bit that is available for external sources of noise is called t_{RNM}. It is the offset from $t_{DJIT(min\ or\ max)}$ for the test mask within the eye opening.

The vertical limits of the mask are determined by the SCAN921260 receiver input threshold of +/− 50mV.

Please refer to the eye mask pattern of *Figure 9* for a graphic representation of t_{DJIT} and t_{RNM}.

$$R_1 = 2R_2 >> R_L$$
$$V_{RL} = 15\,mV$$
$$I_{RL} = 15\,mV/R_L = 3.3V/R_1 + R_2$$
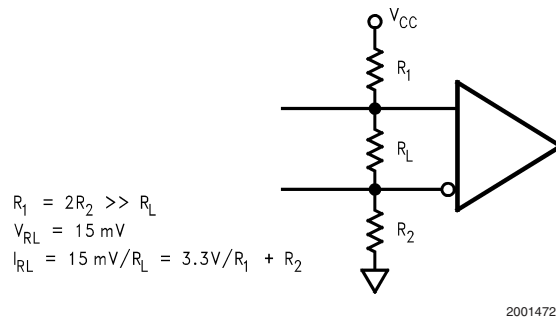
20014727

FIGURE 8. Failsafe Biasing Setup
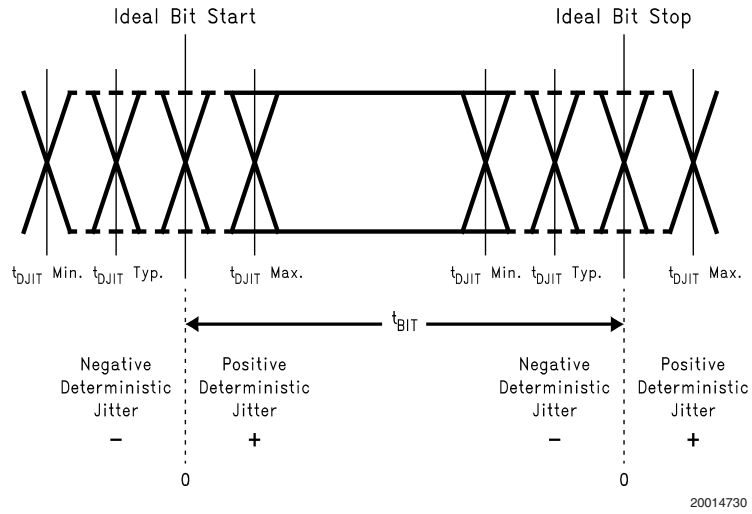
FIGURE 9. Deterministic Jitter and ideal Bit Position

$$\text{Ideal Sampling Position} = \frac{(t_{BIT})}{2}$$

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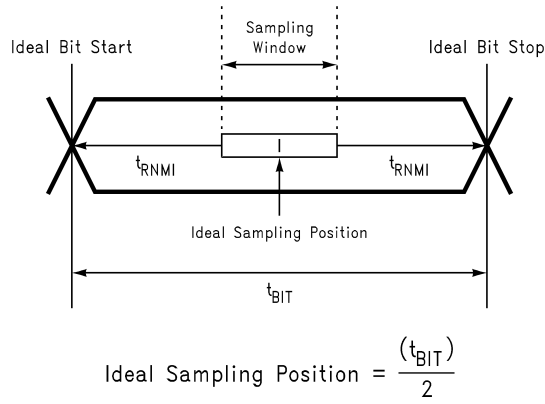
t_{RNMI-L} is the ideal noise margin on the left of the figure, it is a negative value to indicate early with respect to ideal.

t_{RNMI-R} is the ideal noise margin on the right of the above figure, it is a positive value to indicate late with respect to ideal.

FIGURE 10. Ideal Deserializer Noise Margin (t_{RNMI}) and Sampling Window

Pin Diagram

SCAN921260UJB and SCAN921260UJBX (196 pin LBGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DGND	REN	$R_{IN0}-$	$R_{IN0}+$	AGND	$R_{IN2}-$	$R_{IN2}+$	AGND	$R_{IN4}-$	$R_{IN4}+$	AV_{DD}	$R_{IN6}-$	$R_{IN6}+$	PGND
B	DV_{DD}	DGND	DV_{DD}	REF_{CLK}	$\overline{PWRDN}$	AV_{DD}	AGND	AGND	AV_{DD}	BISTMODE_REQ	AGND	PGND	SEL2	DGND
C	TMS	$\overline{TRST}$	CHTST	DV_{DD}	$R_{IN1}-$	$R_{IN1}+$	AV_{DD}	$R_{IN3}-$	$R_{IN3}+$	$R_{IN5}-$	$R_{IN5}+$	SEL0	SEL1	BIST_SEL2
D	TDI	TCK	TDO	DGND	DGND	DV_{DD}	DGND	BIST_SEL0	DGND	PGND	DGND	DV_{DD}	$\overline{LOCK_5}$	BIST_SEL1
E	PV_{DD}	R_{OUT09}	CHTST_EN	R_{OUT08}	DGND	DV_{DD}	DV_{DD}	DGND	DV_{DD}	DV_{DD}	N/C	R_{OUT57}	R_{OUT58}	R_{OUT59}
F	PV_{DD}	$RCLK_0$	$\overline{LOCK_0}$	R_{OUT07}	DGND	DGND	DV_{DD}	PGND	DGND	DV_{DD}	N/C	DV_{DD}	$RCLK_5$	PV_{DD}
G	PGND	PGND	R_{OUT06}	R_{OUT05}	DGND	DV_{DD}	DGND	DGND	DGND	DV_{DD}	R_{OUT55}	R_{OUT56}	PGND	PV_{DD}
H	PGND	R_{OUT04}	R_{OUT02}	R_{OUT03}	DGND	DV_{DD}	DGND	DGND	DGND	DV_{DD}	R_{OUT54}	R_{OUT53}	PGND	PGND
J	PV_{DD}	R_{OUT12}	R_{OUT10}	PGND	DV_{DD}	DGND	DGND	DV_{DD}	DV_{DD}	DV_{DD}	R_{OUT52}	R_{OUT51}	PGND	PV_{DD}
K	PV_{DD}	R_{OUT14}	R_{OUT00}	R_{OUT01}	DV_{DD}	DV_{DD}	DV_{DD}	DGND	DGND	DV_{DD}	BIST_ACT	R_{OUT50}	R_{OUT40}	PV_{DD}
L	R_{OUT13}	$RCLK_1$	R_{OUT11}	N/C	N/C	R_{OUT21}	DGND	R_{OUT31}	R_{OUT34}	DV_{DD}	R_{OUT45}	R_{OUT41}	R_{OUT44}	R_{OUT42}
M	R_{OUT15}	R_{OUT18}	R_{OUT19}	R_{OUT29}	R_{OUT25}	R_{OUT23}	R_{OUT20}	R_{OUT30}	R_{OUT33}	R_{OUT35}	R_{OUT36}	R_{OUT46}	$RCLK_4$	R_{OUT43}
N	R_{OUT16}	R_{OUT17}	$\overline{LOCK_2}$	R_{OUT27}	$RCLK_2$	R_{OUT22}	PGND	PGND	R_{OUT32}	$RCLK_3$	R_{OUT37}	R_{OUT39}	R_{OUT47}	R_{OUT48}
P	$\overline{LOCK_1}$	R_{OUT28}	R_{OUT26}	R_{OUT24}	PV_{DD}	PV_{DD}	PGND	PGND	PV_{DD}	PV_{DD}	R_{OUT38}	$\overline{LOCK_3}$	$\overline{LOCK_4}$	R_{OUT49}

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Pin Descriptions

Pin Name	Type	Pins	Description
SEL (0:2)	CMOS Input	B13, C12, C13	These pins control which Bus LVDS input is steered to the CHTST output. The Control Pins Truth Table describes their function. There are weak internal pull-ups that should default all SEL(0:2) to high. For example, if you choose not to use Channel Test Mode and want the CHTST output permanently disabled, you can tie SEL2 and SEL1 high and SEL0 low. In a noisy operating environment, it is recommended that an external pull up be used to ensure that SELn is in the high state.
Rin +/- n	Bus LVDS Input	A4-A3, A7-A6, A10-A9, A13-A12, C6-C5, C9-C8, C11-C10,	Bus LVDS differential input pins
AGND		A5, A8, B7, B8, B11	Analog Ground
AVDD		A11, B6, B9, C7	Analog Voltage Supply
$\overline{\text{PWRDN}}$	CMOS Input	B5	A low on this pin puts the device into sleep mode and a high makes the part active. There is an internal pull-down that defaults $\overline{\text{PWRDN}}$ to sleep mode. Active operation requires asserting a high on $\overline{\text{PWRDN}}$.
REN	CMOS Input	A2	Enables the Routn and RCLKn outputs. There is an internal pull-down that defaults REN to TRI-STATE the outputs. Active outputs require asserting a high on REN.
REFCLK	CMOS Input	B4	Frequency reference clock input.
CHTST	CMOS Output	C3	Allows low speed testing of the Rin inputs under control of the SEL (0:2) pins.
$\overline{\text{LOCK}}$ (0:5)	CMOS Output	F3, P1, N3, P12, P13, D13	Indicates the status of the PLLs for the individual deserializers: $\overline{\text{LOCK}}$= L indicates locked, $\overline{\text{LOCK}}$= H indicates unlocked.
Rout nx	CMOS Output	E2, E4, E12, E13, E14, F4, G3, G4, G11, G12, H2, H3, H4, H11, H12, J2, J3, J11, J12, K2, K3, K4, K12, K13, L1, L3, L6, L8, L9, L11, L12, L13, L14, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M14, N1, N2, N4, N6, N9, N11, N12, N13, N14, P2, P3, P4, P11, P14	Outputs for the ten bit deserializers, n = deserializer number, x = bit number
RCLK (0:5)	CMOS Output	F2, F13, L2, M13, N5, N10	Recovered clock for each deserializer's output data.
DVDD		B1, B3, C4, D6, D12, E6, E7, E9, E10, F7, F10, F12, G6, G10, H6, H10, J5, J8, J9, J10, K5, K6, K7, K10, L10	Digital Supply Voltage.
DGND		A1, B2, B14, D4, D5, D7, D9, D11, E5, E8, F5, F6, F9, G5, G7, G8, G9, H5, H7, H8, H9, J6, J7, K8, K9, L7	Digital Ground.
PVDD		E1, F1, F14, G14, J1, J14, K1, K14, P5, P6, P9, P10	PLL Supply Voltage.
PGND		A14, B12, D10, F8, G1, G2, G13, H1, H13, H14, J4, J13, N7, N8, P7, P8	PLL Ground.

Pin Descriptions (Continued)

Pin Name	Type	Pins	Description
TMS	CMOS Input	C1	Test Mode Select input to support IEEE 1149.1
TRST	CMOS Input	C2	Test Reset Input to support IEEE 1149.1
TDI	CMOS Input	D1	Test Data Input to support IEEE 1149.1
TCK	CMOS Input	D2	Test Clock to support IEEE 1149.1
TDO	CMOS Output	D3	Test Data Output to support TDO
BISTMODE_REQ	CMOS Input	B10	BIST Alone Error Reporting Mode Select Input
BIST_SEL(0:2)	CMOS Input	C14, D8, D14	These pins control which channels are active for the BIST Alone operation mode. The BIST Alone Mode Selection Table describes their function. There are internal pull-ups that default all BIST_SEL(0:2) to high, which is the idle state for all channels in BIST Alone mode.
CHTST_EN	CMOS Input	E3	A high on this input enables the CHTST output. There is an internal pull-up that defaults the CHTST output to the active mode. Note: CHTEST_EN requires two clock cycles before CHTST is enabled or disabled. When not using CHTST output, assert a low on this control pin to reduce power consumption.
BIST_ACT	CMOS Input	K11	A high on this pin activates the BIST Alone operating mode. There is a weak internal pull-down that should default the BIST_ACT to de-activate the BIST Alone operating mode. In a noisy operating environment, it is recommended that an external pull down be used to ensure that BIST_ACT is in the low state.
N/C		E11, F11, L4, L5	Unused solder ball location. Do not connect.

Physical Dimensions inches (millimeters) unless otherwise noted
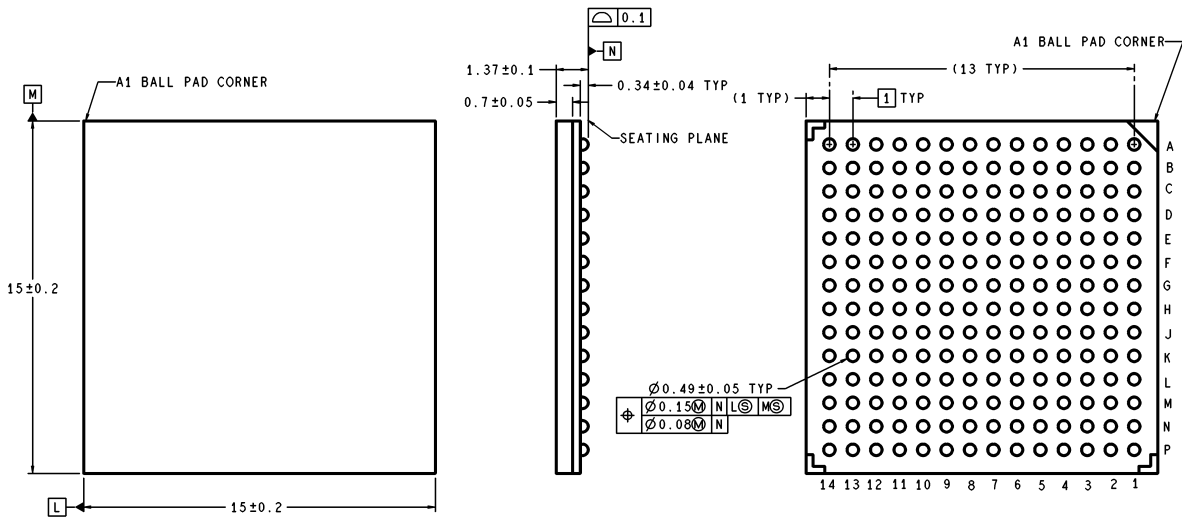
DIMENSIONS ARE IN MILLIMETERS

UJB196A (Rev B)

Order Number SCAN921260UJB (Tray)
Order Number SCAN921260UJBX (Tape and Reel)
NS Package Number UJB196A

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